

SPECIFICATION

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[EXTRUSION-FREE WET CLEANING PROCESS FOR COPPER-DUAL DAMASCENE STRUCTURES]

Background of Invention

[0001] 1.Field of the Invention

[0002] The present invention relates to an improved wet cleaning approach to back-end of line (BEOL) processes. More particularly, the present invention relates to an improved two-step wet cleaning process incorporated with an extrusion inhibition step for post-etch copper structures, particularly, for copper-dual damascene structures. The two-step wet cleaning process comprises a mild oxidation step followed by an oxide etch step. This approach demonstrates clean copper dual damascene structures having no copper extrusions that arise due to oxidation-reduction ("redox") reactions in a wet cleaning solution abundant in dissolved copper ions.

[0003] 2.Description of the Prior Art

[0004] Aluminum alloys with SiO_2 dielectrics have been the materials of choice for interconnect systems since the dawn of the integrated circuit (IC) era. These materials were convenient to process using mature subtractive etch processes for metal line patterning. However, as ICs have relentlessly marched down the path towards smaller geometry in the pursuit of increased speed and integration density, the traditional Al/SiO_2 interconnect system has shown itself to be a limiting factor. Cu-dual damascene architectures with low-k dielectrics are thus

developing and becoming the norm now in forming interconnects in the BEOL processes.

[0005] Although Cu/low-k materials present many benefits from a circuit perspective, they require an entirely new process technology for interconnect fabrication. Fortunately, many of these process issues have been addressed with intermediate interconnect systems employing Cu metal with low-k dielectrics. Some of these low-k materials include FLARETM, SiLKTM and BCB (porous dielectrics). This Cu/low-k material process flow led to the development of Cu dual damascene processes in order to overcome the difficulties presented with reactive ion etching (RIE) of Cu. However, processing with these Cu/low-k material systems presents an entirely new set of problems that must be overcome. Etching vias and trenches results in the formation of complex organometallic polymers, which are difficult to clean using dry processes. Since Cu does not possess the self-passivating properties of Al, the tendency of Cu to corrode when exposed to an oxidizing environment is also a major concern. This is especially problematic with the wet immersion processes required for cleaning Cu/low-k etch residues.

[0006] One approach typically used to clean copper structures after via/trench dry etch is using a very diluted aqueous HF-based cleaning process. An alternative approach featuring its effectiveness, which was developed by Mattson Technology Wet Process Division (Exton, Pa.) and United Microelectronics Corp. (Hsinchu, Taiwan), includes a two-step process based on the diluted HF-based cleaning process. The first step of the two-step process is a mild oxidation step consisting of a dilute H₂O₂ solution 36:1 and a surfactant with megasonics irradiation. This step removes some polymer residues and the sputtered Cu on the sidewalls of the vias and trenches, and oxidizes the copper surface. The first step can be used without a surfactant. The second step is a mild oxide etch utilizing dilute HF, NH₄F or NH₂OH. This step undercuts the polymer residues and removes both leftover sputtered copper from the sidewalls, and oxide, such as CuO_x and Cu(OH)₂, from the copper surface.

[0007]

Referring now to Fig.1 of a post-etch dual damascene structure 30 formed on a

silicon substrate 10, in an acidic ambient, such as HF solution, the lift CuO_x and $\text{Cu}(\text{OH})_2$ molecules dissolve and thus produce massive copper ions (Cu^{2+}) in the solution (see eq.1). In Fig.1, after dipping the silicon substrate 10 into an acidic oxide etch solution for a certain time period, a recess 13 formed due to the Cu loss is observed at a top surface of a metal-1 (M-1), i.e. first level metal, Cu wiring line 22 which is electrically connected with a P^+ diffusion region 12 of the silicon substrate 10 via a tungsten plug 16. In the meantime, an undesirable extrusion 15 is formed atop an adjacent M-1 Cu wiring line 24 which is electrically connected with a N^+ diffusion (electron-rich) region 12 of the silicon substrate 10 via a tungsten plug 18. A reasonable explanation for this phenomenon is that the P-N junction fabricated in the silicon substrate 10 provides an electrical path for electrochemical reactions. Excessive copper ions deposit on the anode (i.e. N^+ region connected Cu wiring line) due to reduction reaction (see eq.2). In the reduction of cupric oxide the oxidation number of copper has changed from +2 to zero by the gain of two electrons.

Summary of Invention

- [0008] It is therefore a primary objective of the present invention to provide an improved post-etch dual damascene wet cleaning process to alleviate the above-mentioned extrusion problems.
- [0009] According to the preferred embodiment, the present invention provides an extrusion-free wet cleaning process for post-etch Cu-dual damascene structures. The process comprises the following steps:
- [0010] (1).providing a wafer comprising a silicon substrate and at least one post-etch Cu-dual damascene structure, the post-etch Cu-dual damascene structure having a via structure exposing a portion of a Cu wiring line electrically connected with an N^+ diffusion region of the silicon substrate, and a trench structure formed on the via structure;
- [0011] (2).applying a diluted H_2O_2 solution on the wafer to slightly oxidize the surface of the exposed Cu wiring line;

[0012] (3).washing away cupric oxide generated in the oxidation step by means of an acidic cupric oxide cleaning solution containing diluted HF, NH_4F or NH_2OH ; and

[0013] (4).providing means for preventing Cu reduction reactions on the Cu wiring line.

[0014] According to one aspect of the present invention, the method of preventing Cu reduction reactions on the Cu wiring line is purging the wafer with inert gas during the wash of wafer by the diluted H_2O_2 solution.

[0015] According to another aspect of the present invention, the method of preventing Cu reduction reactions on the Cu wiring line is adding a Cu corrosion inhibitor such as benzotriazole (BTA) into the diluted H_2O_2 solution.

[0016] According to another aspect of the present invention, the method of preventing Cu reduction reactions on the Cu wiring line is reducing the H_2O_2 concentration of the diluted H_2O_2 solution to below 100:1 (v/v).

[0017] According to another aspect of the present invention, the method of preventing Cu reduction reactions on the Cu wiring line is lowering the temperature of the diluted H_2O_2 solution during the wash of the wafer to below 15 °C.

[0018] According to another aspect of the present invention, the method of preventing Cu reduction reactions on the Cu wiring line is increasing the pH of the acidic cupric oxide cleaning solution to above 7.

[0019] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the various figures and drawings.

Brief Description of Drawings

[0020]

Fig.1 is a cross-sectional diagram schematically showing a Cu-dual damascene interconnect structure after performing a wet cleaning process according to the

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prior art.

[0021] Fig.2 is schematic dual damascene interconnect structure used to evaluate the efficacy of the improved post-etch cleaning treatments on dual damascene etch residues according to the present invention.

[0022] Fig.3 is a flow chart depicting extrusion inhibition improvement steps according to the present invention.

Detailed Description

[0023] Dual damascene structures 90 used to evaluate the efficacy of improved post-etch cleaning treatments on dual damascene etch residues according to the present invention are now illustrated in Fig.2. The post-etch dual damascene structures 90 are representative of a dual damascene process flow for a two-level Cu metal system with low-k dielectric layers 72. A wide range of both inorganic and organic low-k ($k < 3$) dielectric materials, produced either by spin-on or CVD processes, are suitable for the present invention. Examples of such inorganic low-k materials include doped oxide: F-doped as FSG; H doped as HSQ; C and H doped as MSQ, HOSP, Black Diamond, Coral and porous silica: aerogels, xerogels and nanoglass. The low-k organic polymers include amorphous fluorocarbon polymers, fluorinated polyimide, PTFE, poly(arylene ether), benzocyclobutene, SilkTM and FLARETM.

[0024] As shown in Fig.2, key features of the dual damascene structures 90 include the use of nitride etch stop layers 82, and oxide hardmasks 84 for patterning the low-k dielectric layers 72. Each dual damascene structure 90, which exposes a portion of the underlying M-1 wiring line 92 and 94, includes a trench, and a via formed beneath the trench. After the etch of the dual damascene structures 90, the via/trench sidewalls show clear evidence of C, O, Si, Cu, and N elemental residues. As mentioned, it is evident that the most problematic cleaning is the M-1 wiring line 94 electrically connected with an N⁺ region 64 of a silicon substrate 60 via a tungsten plug 68.

[0025] To inhibit Cu reduction reactions that occur over the M-1 wiring line 94 and

thus resolve the Cu extrusion due to Cu reduction reactions, means for preventing Cu reduction reactions on the Cu wiring line are added to the two-step wet cleaning process. The improved wet process includes the following steps:

[0026] (1)oxidation step;

[0027] (2)oxide etch step; and

[0028] (3)extrusion inhibition step;

[0029] wherein the oxidation step is a mild oxidation step consisting of a dilute H_2O_2 solution and a surfactant with megasonics irradiation. This step removes some polymer residues and the sputtered Cu on the sidewalls of the vias and trenches, and slightly oxidizes the copper surface. The first step can be used without a surfactant. The second step is a mild oxide etch with an etchant containing dilute HF/HCl, HF, NH_4F or NH_2OH . This step undercuts the polymer residues and removes both leftover sputtered copper from the sidewalls and oxide such as CuO_x and $Cu(OH)_2$ from the copper surface. The extrusion inhibition step can be applied during either the oxidation step or the oxide etch step, or, both the oxidation step and the oxide etch step. The goal of the extrusion inhibition step is to prevent cupric ions dissolved in the oxide etch solution from depositing on the exposed surface of the M-1 wiring line 94.

[0030]

Please refer to Fig.3, which is a flow chart depicting the extrusion inhibition improvement steps according to the present invention. As shown in Fig.3, in a preferred embodiment of the present invention, there are four choices of extrusion inhibition means, which are subject to the oxidation step. They are (1) purging a wafer with inert gas during the wash of the wafer by the diluted H_2O_2 solution; (2) adding a Cu corrosion inhibitor such as benzotriazole (BTA) into the diluted H_2O_2 solution; (3) reducing the H_2O_2 concentration of the diluted H_2O_2 solution to below 100:1 (v/v); and (4) lowering the temperature of the diluted H_2O_2 solution during the wash of the wafer by the diluted H_2O_2 solution to below 15 °C. The four choices can be used alone or used by combining two, three, or all of the choices. There is one improvement step in the preferred embodiment for

inhibiting Cu reduction reactions on the M-1 wiring line 94. The suggested inhibition step, which is subject to the oxide etch step, is increasing the pH of the acidic cupric oxide cleaning solution to above 7, or using alkaline oxide cleaning solutions known in the art. The inhibition step which is subject to the oxide etch step can be used in combination with the choices being subject to the oxidation step.

[0031] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

FIG. 20